

**Quad, 125MHz Video  
Current Feedback Amplifier**

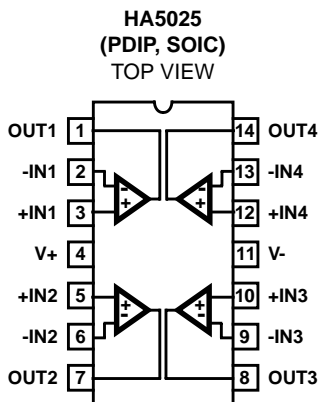
The HA5025 is a wide bandwidth high slew rate quad amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor.

The performance of the HA5025 is very similar to the popular Intersil HA-5020.

**Pinout**



**Features**

- Wide Unity Gain Bandwidth . . . . . 125MHz
- Slew Rate . . . . . 475V/μs
- Input Offset Voltage . . . . . 800μV
- Differential Gain . . . . . 0.03%
- Differential Phase . . . . . 0.03 Degrees
- Supply Current (per Amplifier) . . . . . 7.5mA
- ESD Protection . . . . . 4000V
- Guaranteed Specifications at ±5V Supplies

**Applications**

- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA5025IP	-40 to 85	14 Ld PDIP	E14.3
HA5025IB	-40 to 85	14 Ld SOIC	M14.15
HA5025EVAL	High Speed Op Amp DIP Evaluation Board		

**Absolute Maximum Ratings**

Voltage Between V+ and V- Terminals . . . . . 36V  
 DC Input Voltage (Note 3) . . . . . ±V<sub>SUPPLY</sub>  
 Differential Input Voltage . . . . . 10V  
 Output Current (Note 4) . . . . . Short Circuit Protected  
 ESD Rating (Note 3)  
 Human Body Model (Per MIL-STD-883 Method 3015.7) . . . . . 2000V

**Thermal Information**

Thermal Resistance (Typical, Note 2) θ<sub>JA</sub> (°C/W)  
 PDIP Package . . . . . 100  
 SOIC Package . . . . . 120  
 Maximum Junction Temperature (Note 1) . . . . . 175°C  
 Maximum Junction Temperature (Plastic Package, Note 1) . . . . . 150°C  
 Maximum Storage Temperature Range . . . . . -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) . . . . . 300°C  
 (SOIC - Lead Tips Only)

**Operating Conditions**

Temperature Range . . . . . -40°C to 85°C  
 Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTES:**

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175°C for die, and below 150°C for plastic packages. See Application Information section for safe operating area information.
2. θ<sub>JA</sub> is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

**Electrical Specifications** V<sub>SUPPLY</sub> = ±5V, R<sub>F</sub> = 1kΩ, A<sub>V</sub> = +1, R<sub>L</sub> = 400Ω, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
<b>INPUT CHARACTERISTICS</b>							
Input Offset Voltage (V <sub>IO</sub> )		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V <sub>IO</sub> Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	µV/°C
V <sub>IO</sub> Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V <sub>IO</sub> Power Supply Rejection Ratio	±3.5V ≤ V <sub>S</sub> ≤ ±6.5V	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection (+I <sub>BCMR</sub> = $\frac{1}{+R_{IN}}$ )	Note 5	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	±3.5V ≤ V <sub>S</sub> ≤ ±6.5V	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25, 85	-	4	12	µA
		A	-40	-	10	30	µA
Delta - IN BIAS Current Between Channels		A	25, 85	-	6	15	µA
		A	-40	-	10	30	µA
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection	±3.5V ≤ V <sub>S</sub> ≤ ±6.5V	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	nV/√Hz

# HA5025

**Electrical Specifications**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 1k\Omega$ ,  $A_V = +1$ ,  $R_L = 400\Omega$ ,  $C_L \leq 10pF$ ,  
Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	pA/√Hz
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	pA/√Hz
<b>TRANSFER CHARACTERISTICS</b>							
Transimpedance	Note 11	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$ , $V_{OUT} = \pm 2.5V$	A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$ , $V_{OUT} = \pm 2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
<b>OUTPUT CHARACTERISTICS</b>							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm 2.5V$ , $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
<b>POWER SUPPLY CHARACTERISTICS</b>							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
<b>AC CHARACTERISTICS</b> ( $A_V = +1$ )							
Slew Rate	Note 6	B	25	275	350	-	V/μs
Full Power Bandwidth	Note 7	B	25	22	28	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns
<b>AC CHARACTERISTICS</b> ( $A_V = +2$ , $R_F = 681\Omega$ )							
Slew Rate	Note 6	B	25	-	475	-	V/μs
Full Power Bandwidth	Note 7	B	25	-	26	-	MHz
Rise Time	Note 8	B	25	-	6	-	ns
Fall Time	Note 8	B	25	-	6	-	ns
Propagation Delay	Note 8	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
<b>AC CHARACTERISTICS</b> ( $A_V = +10$ , $R_F = 383\Omega$ )							
Slew Rate	Note 6	B	25	350	475	-	V/μs
Full Power Bandwidth	Note 7	B	25	28	38	-	MHz

**Electrical Specifications**  $V_{SUPPLY} = \pm 5V$ ,  $R_F = 1k\Omega$ ,  $A_V = +1$ ,  $R_L = 400\Omega$ ,  $C_L \leq 10pF$ , Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 9) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Rise Time	Note 8	B	25	-	8	-	ns
Fall Time	Note 8	B	25	-	9	-	ns
Propagation Delay	Note 8	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
<b>VIDEO CHARACTERISTICS</b>							
Differential Gain (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 10)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

- $V_{CM} = \pm 2.5V$ . At  $-40^\circ C$  Product is tested at  $V_{CM} = \pm 2.25V$  because Short Test Duration does not allow self heating.
- $V_{OUT}$  switches from  $-2V$  to  $+2V$ , or from  $+2V$  to  $-2V$ . Specification is from the 25% to 75% points.
- $FPBW = \frac{Slew\ Rate}{2\pi V_{PEAK}}$ ;  $V_{PEAK} = 2V$ .
- $R_L = 100\Omega$ ,  $V_{OUT} = 1V$ . Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
- A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
- Measured with a VM700A video tester using an NTC-7 composite VITS.
- $V_{OUT} = \pm 2.5V$ . At  $-40^\circ C$  Product is tested at  $V_{OUT} = \pm 2.25V$  because Short Test Duration does not allow self heating.

**Test Circuits and Waveforms**

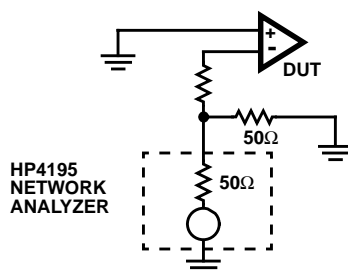


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

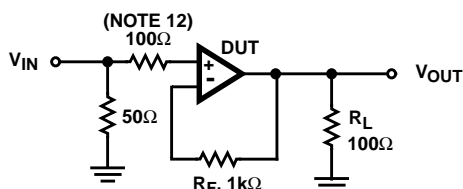


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

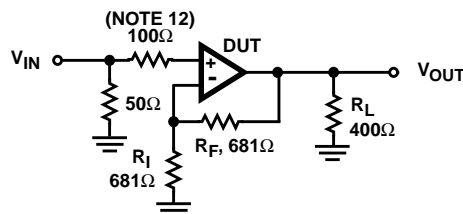
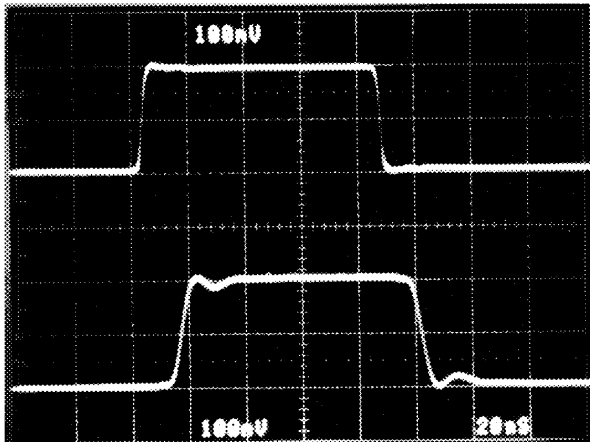


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

NOTE:

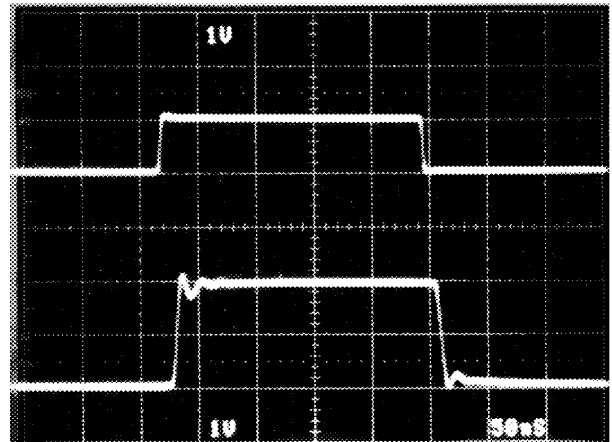
- A series input resistor of  $\geq 100\Omega$  is recommended to limit input currents in case input signals are present abefore the HA5025 is powered up.

Test Circuits and Waveforms (Continued)



Vertical Scale:  $V_{IN} = 100\text{mV/Div.}$ ,  $V_{OUT} = 100\text{mV/Div.}$   
Horizontal Scale: 20ns/Div.

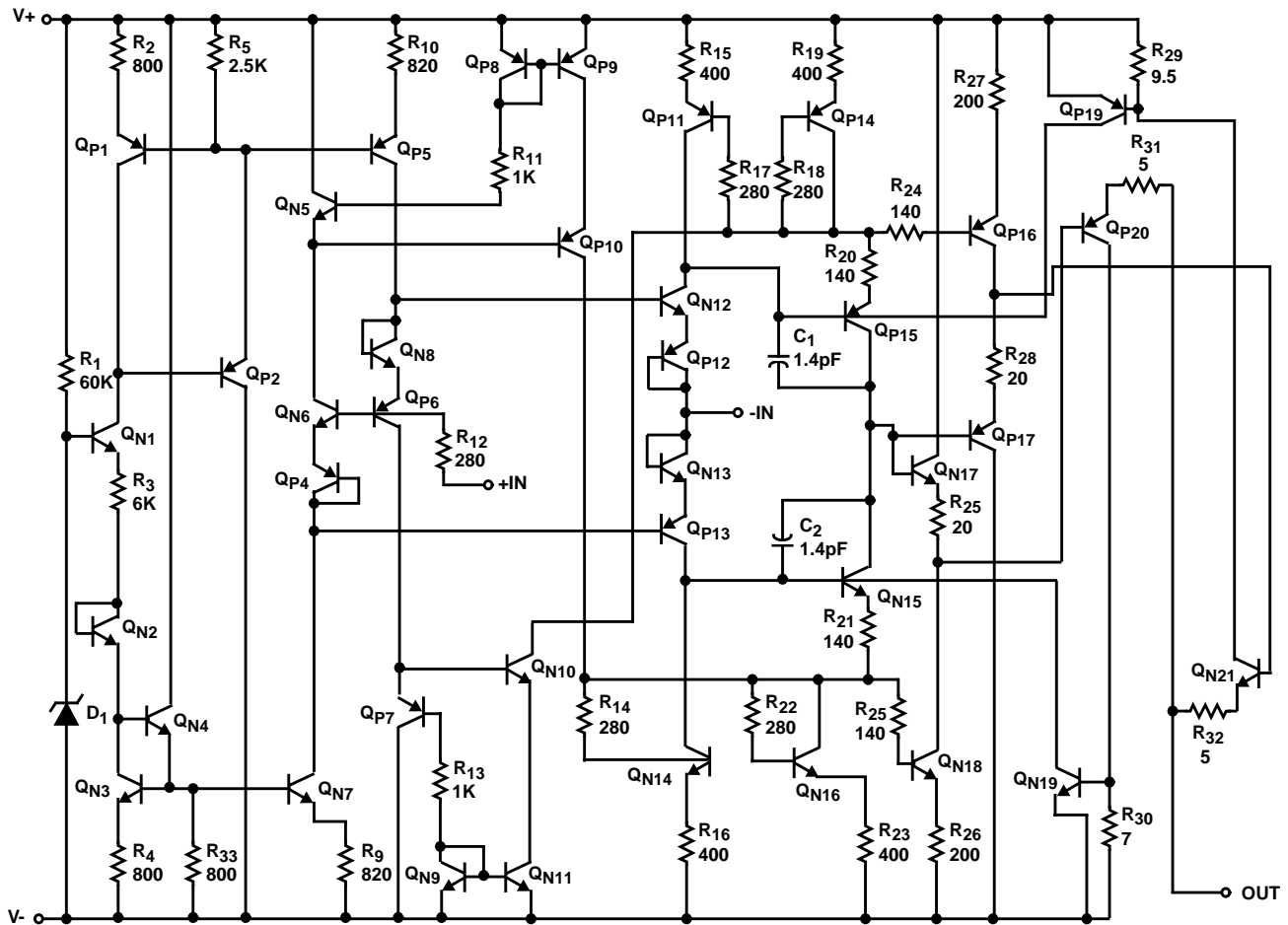
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale:  $V_{IN} = 1\text{V/Div.}$ ,  $V_{OUT} = 1\text{V/Div.}$   
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic Diagram (One Amplifier of Four)



## Application Information

### Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5025 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and  $R_F$ . All current feedback amplifiers require a feedback resistor, even for unity gain applications, and  $R_F$ , in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to  $R_F$ . The HA5025 design is optimized for a  $1000\Omega$   $R_F$  at a gain of +1. Decreasing  $R_F$  in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so  $R_F$  can be decreased in a trade-off of stability for bandwidth.

The following table lists recommended  $R_F$  values for various gains, and the expected bandwidth.

GAIN (A <sub>CL</sub> )	R <sub>F</sub> (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

### PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value ( $10\mu\text{F}$ ) tantalum or electrolytic capacitor in parallel with a small value ( $0.1\mu\text{F}$ ) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to

-IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

### Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

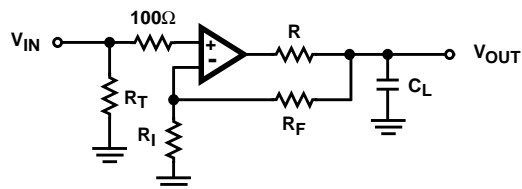


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but  $27\Omega$  has been determined to be a good starting value.

### Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature ( $T_J$ , see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (PDIP, SOIC). At  $V_S = \pm 5\text{V}$  quiescent operation both package styles may be operated over the full industrial range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . It is recommended that thermal calculations, which take into account output power, be performed by the designer.

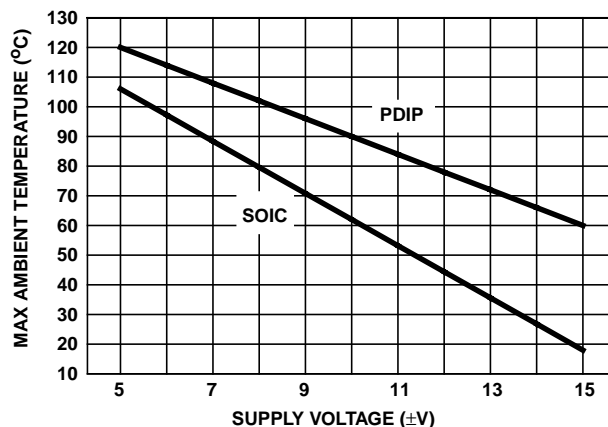


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified

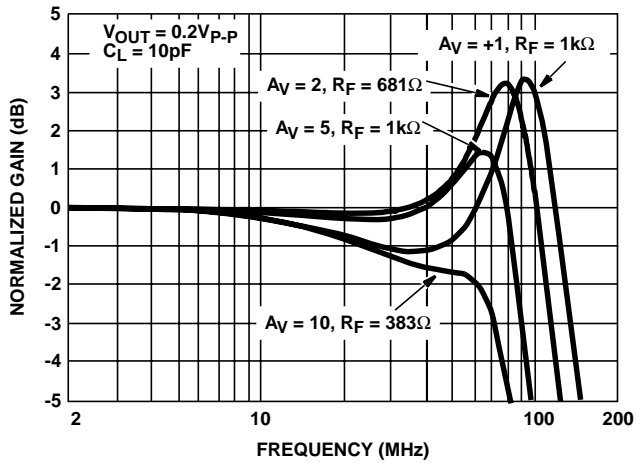


FIGURE 8. NON-INVERTING FREQUENCY RESPONSE

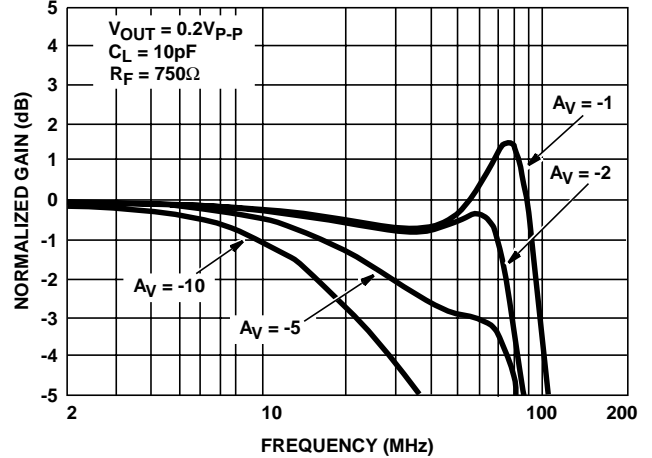


FIGURE 9. INVERTING FREQUENCY RESPONSE

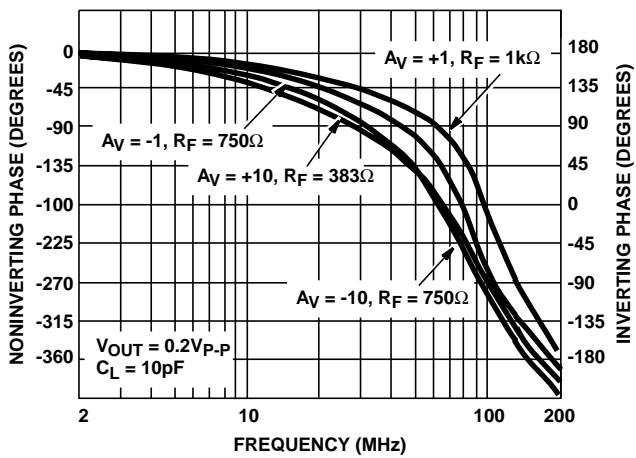


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

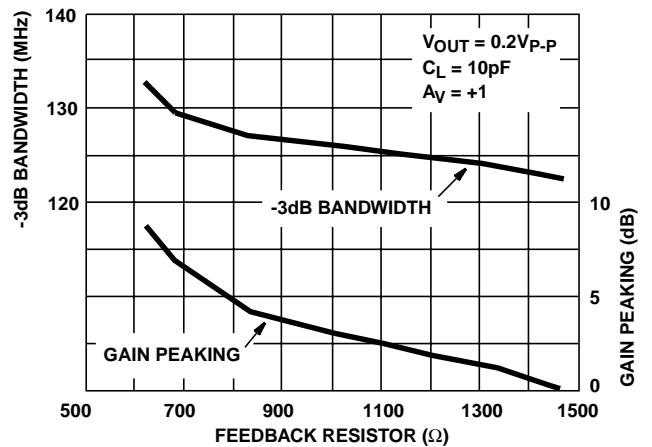


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

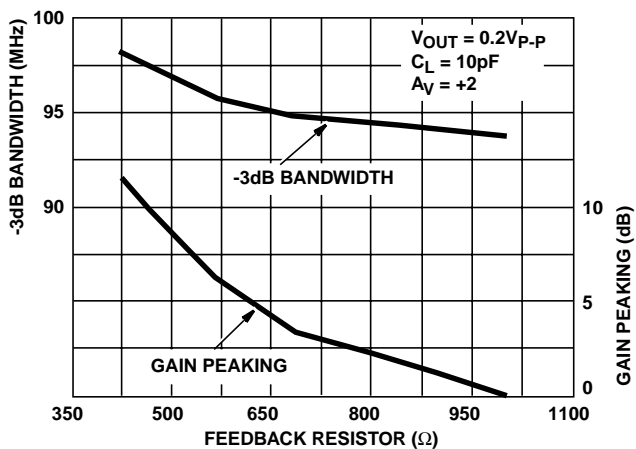


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

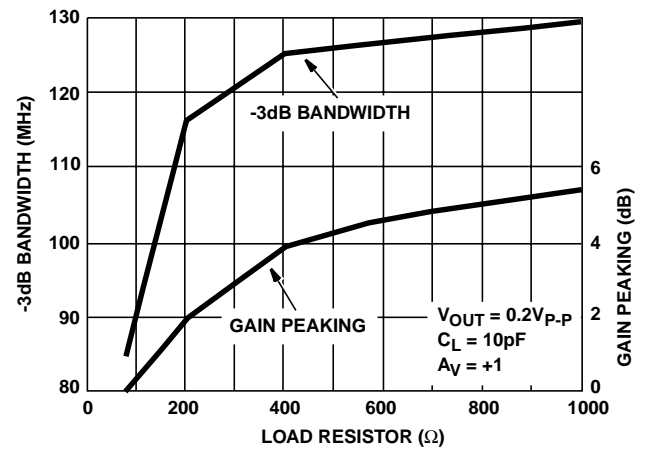


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified (Continued)

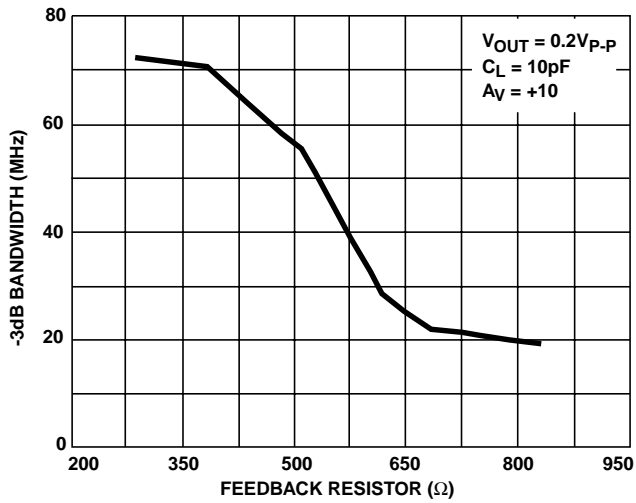


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

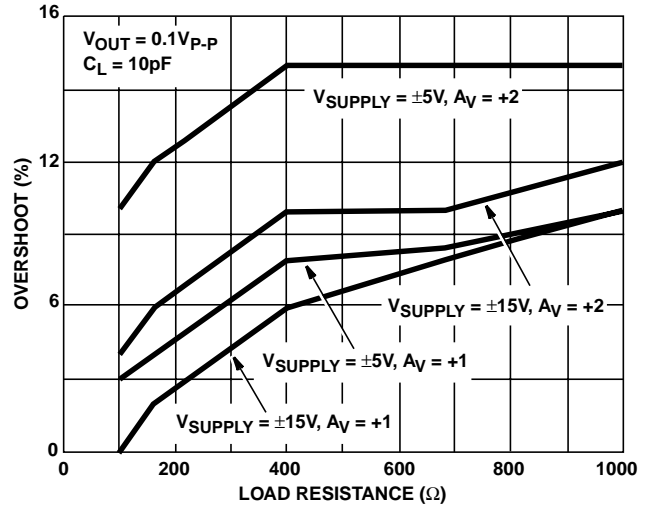


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

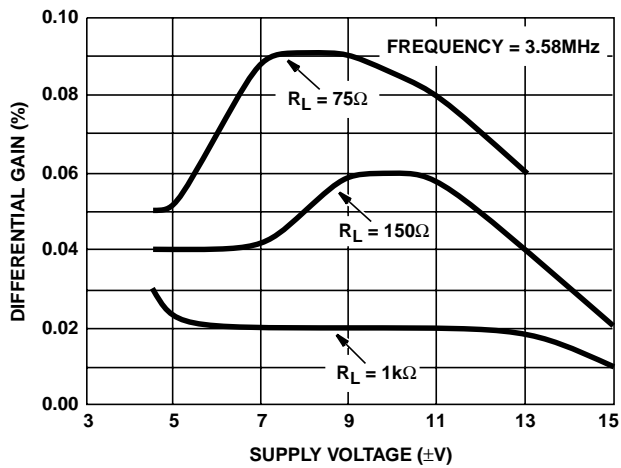


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

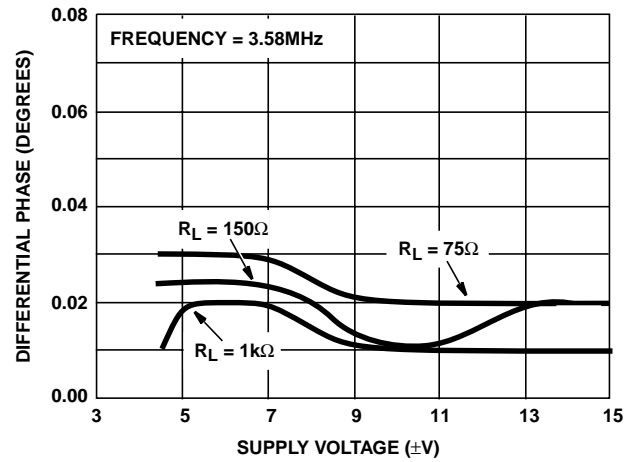


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

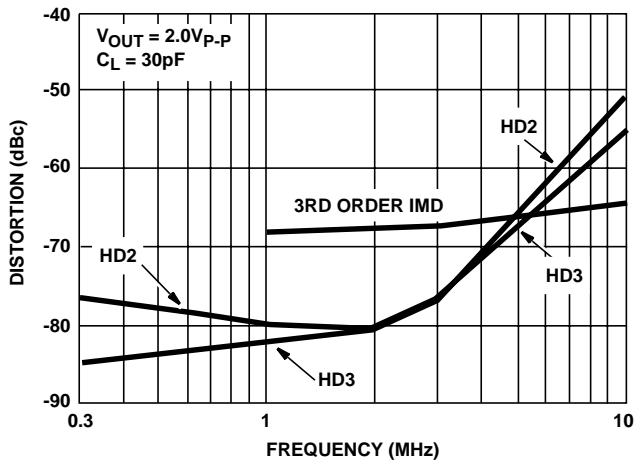


FIGURE 18. DISTORTION vs FREQUENCY

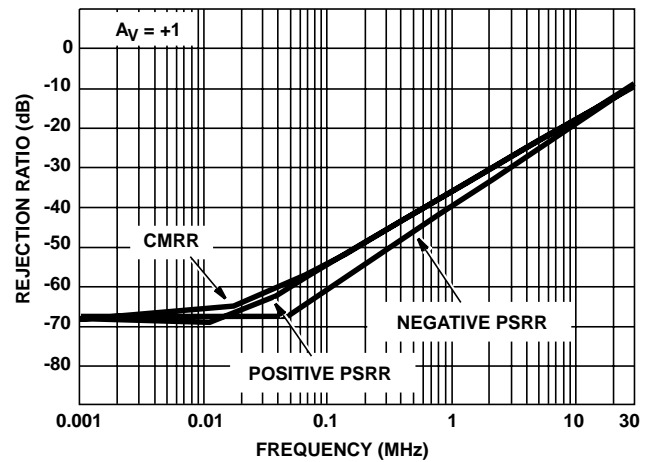


FIGURE 19. REJECTION RATIOS vs FREQUENCY



**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified (Continued)

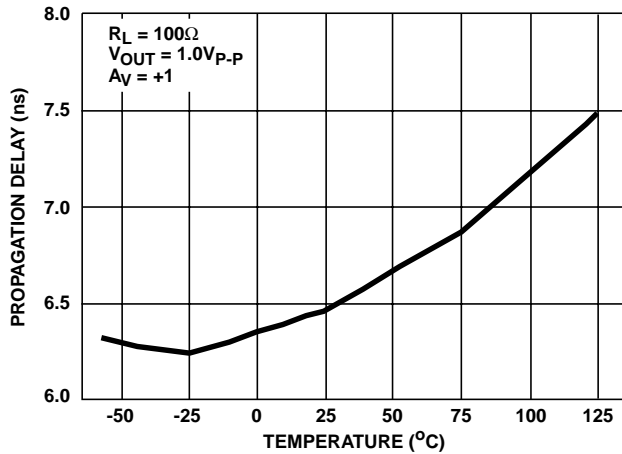


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

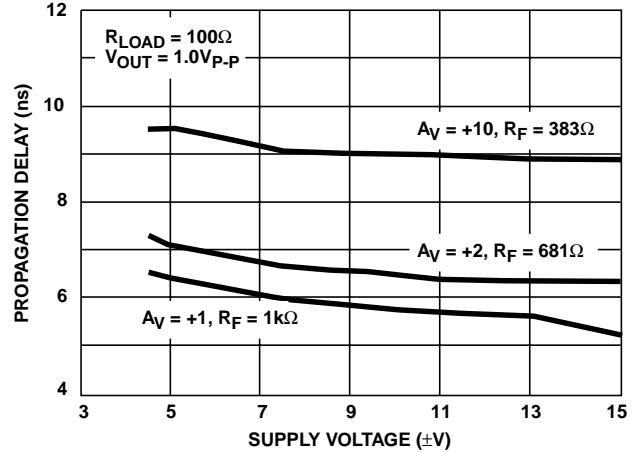


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

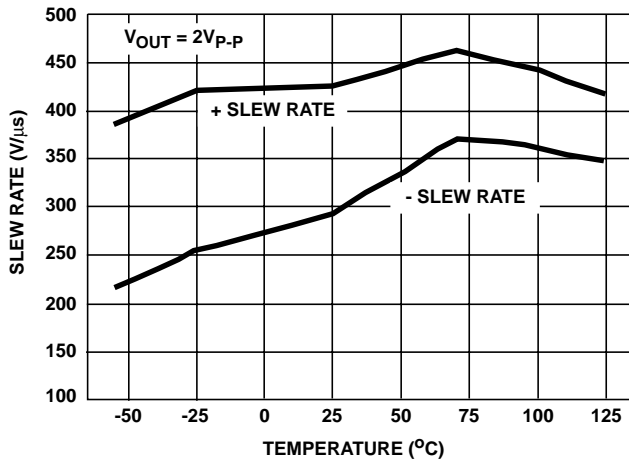


FIGURE 22. SLEW RATE vs TEMPERATURE

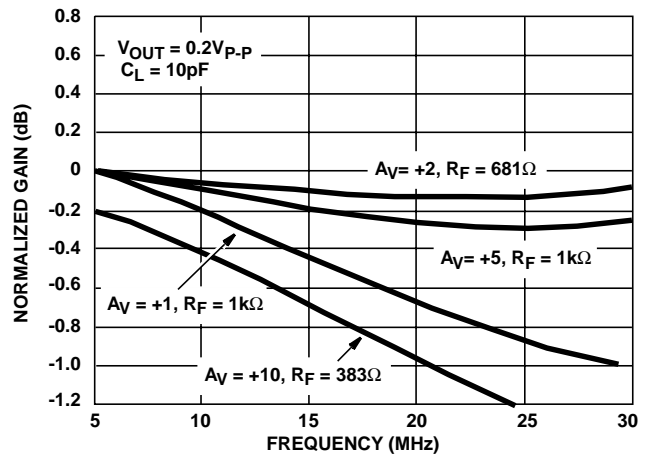


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

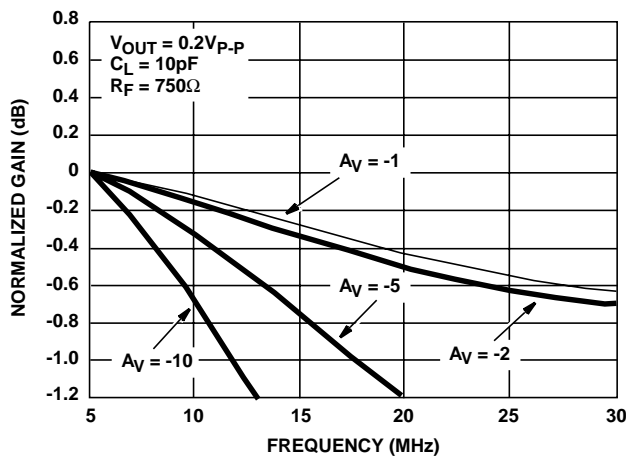


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

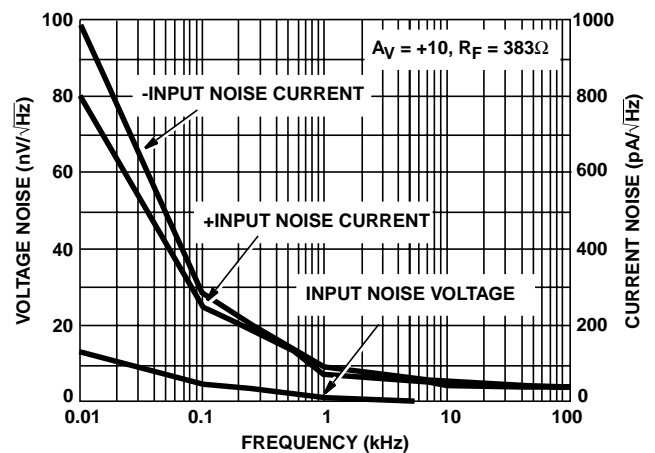


FIGURE 25. INPUT NOISE CHARACTERISTICS

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified (Continued)

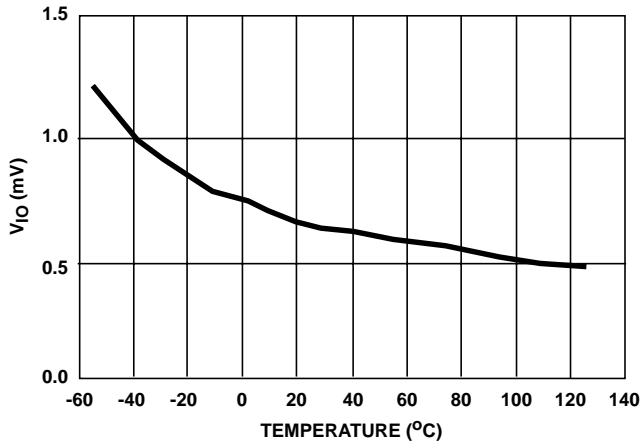


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

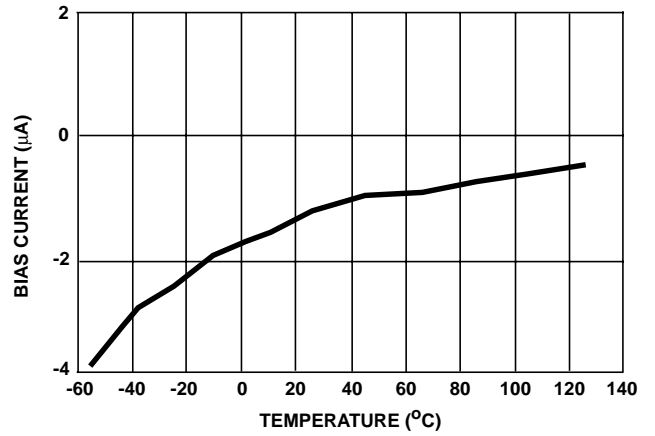


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

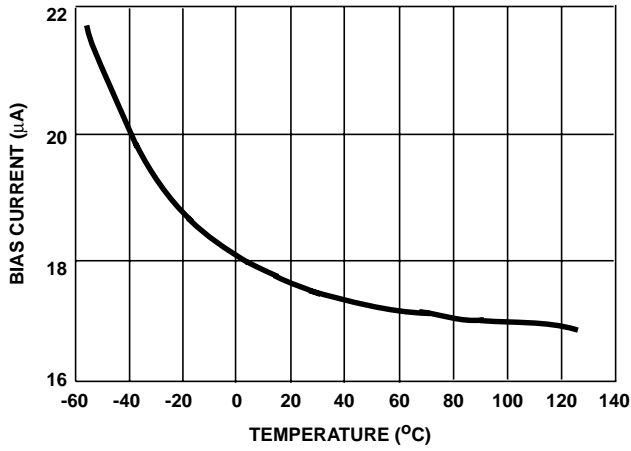


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

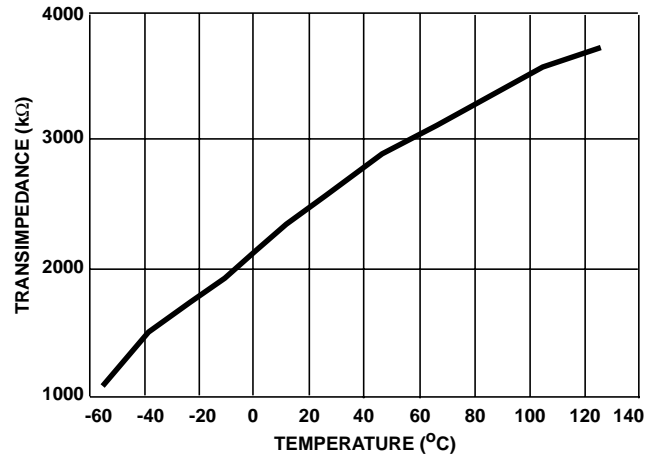


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

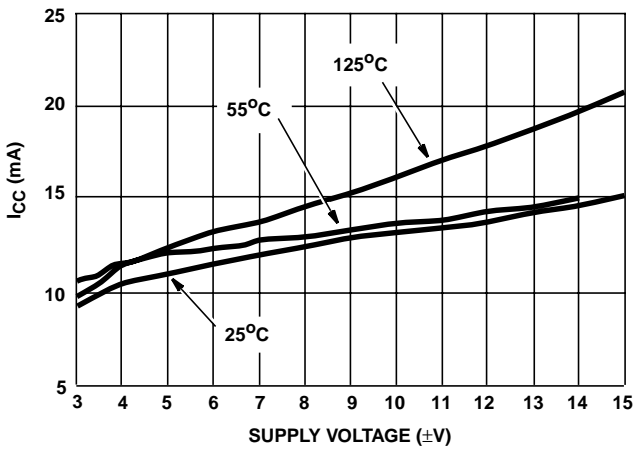


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

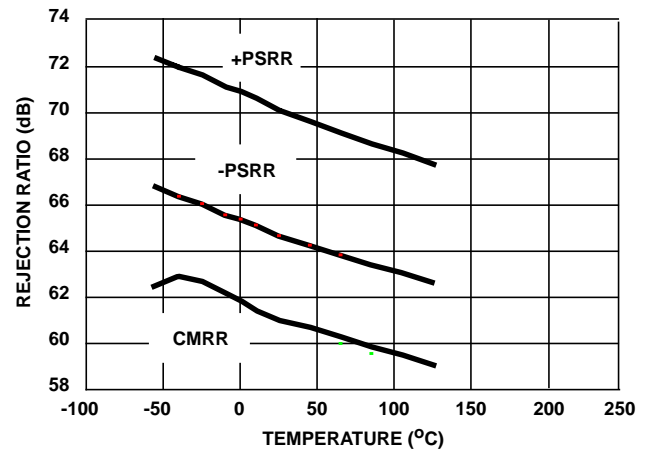


FIGURE 31. REJECTION RATIO vs TEMPERATURE

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified (Continued)

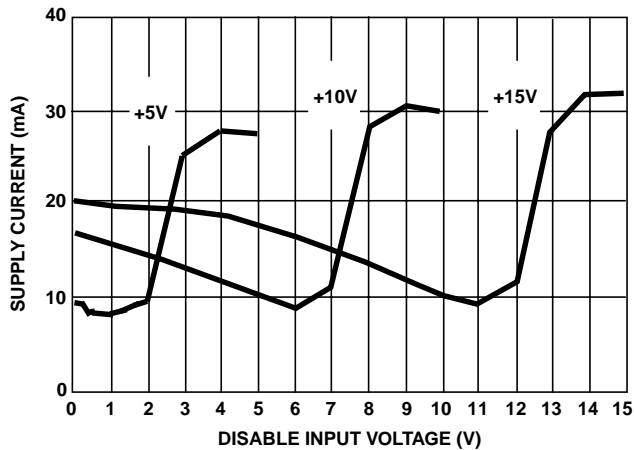


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

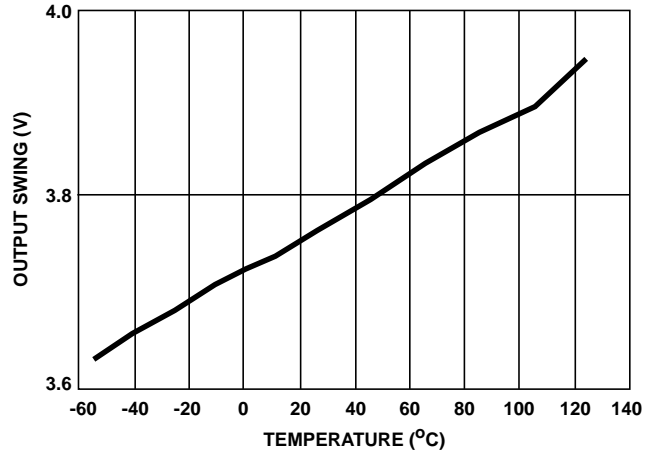


FIGURE 33. OUTPUT SWING vs TEMPERATURE

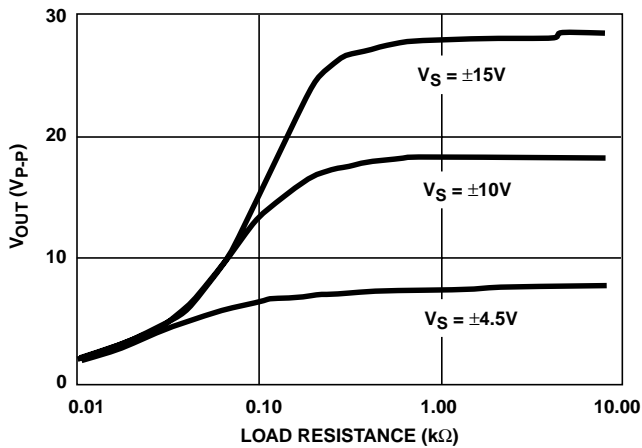


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

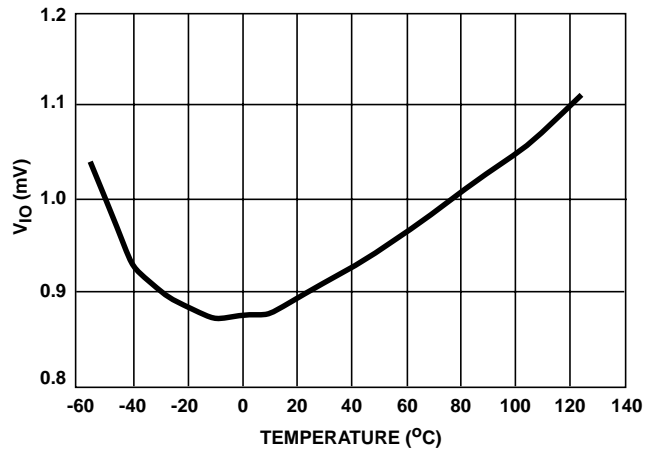


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

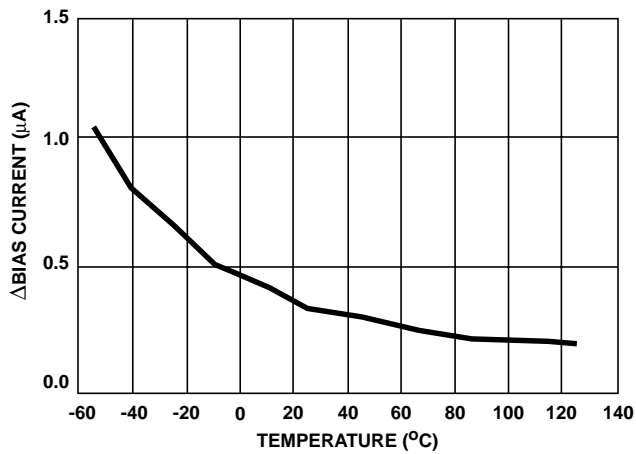


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

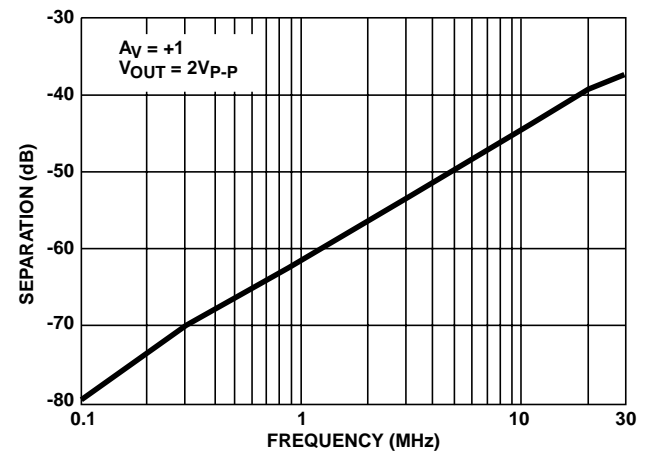


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

**Typical Performance Curves**  $V_{SUPPLY} = \pm 5V$ ,  $A_V = +1$ ,  $R_F = 1k\Omega$ ,  $R_L = 400\Omega$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified (Continued)

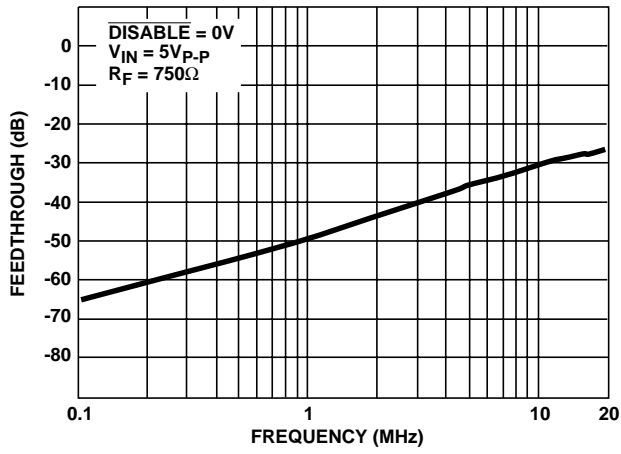


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

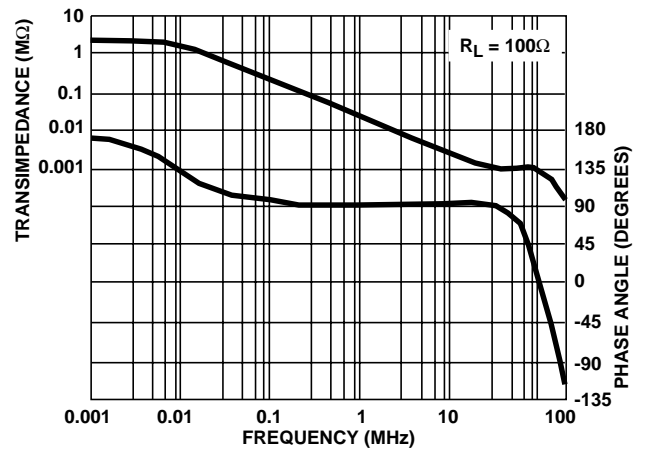


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

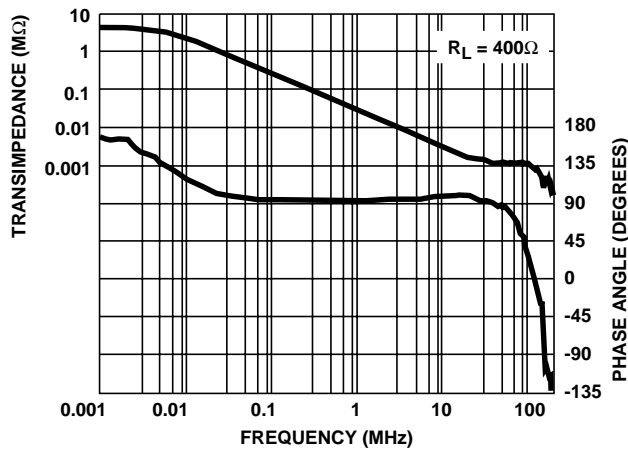


FIGURE 40. TRANSIMPEDANCE vs FREQUENCY

**Die Characteristics**

**DIE DIMENSIONS:**

2010µm x 3130µm x 483µm

**METALLIZATION:**

Type: Metal 1: AlCu (1%)

Thickness: Metal 1: 8kÅ ±0.4kÅ

Metal 2: AlCu (1%)

Metal 2: 16kÅ ±0.8kÅ

**PASSIVATION:**

Type: Nitride

Thickness: 4kÅ ±0.4kÅ

**TRANSISTOR COUNT:**

248

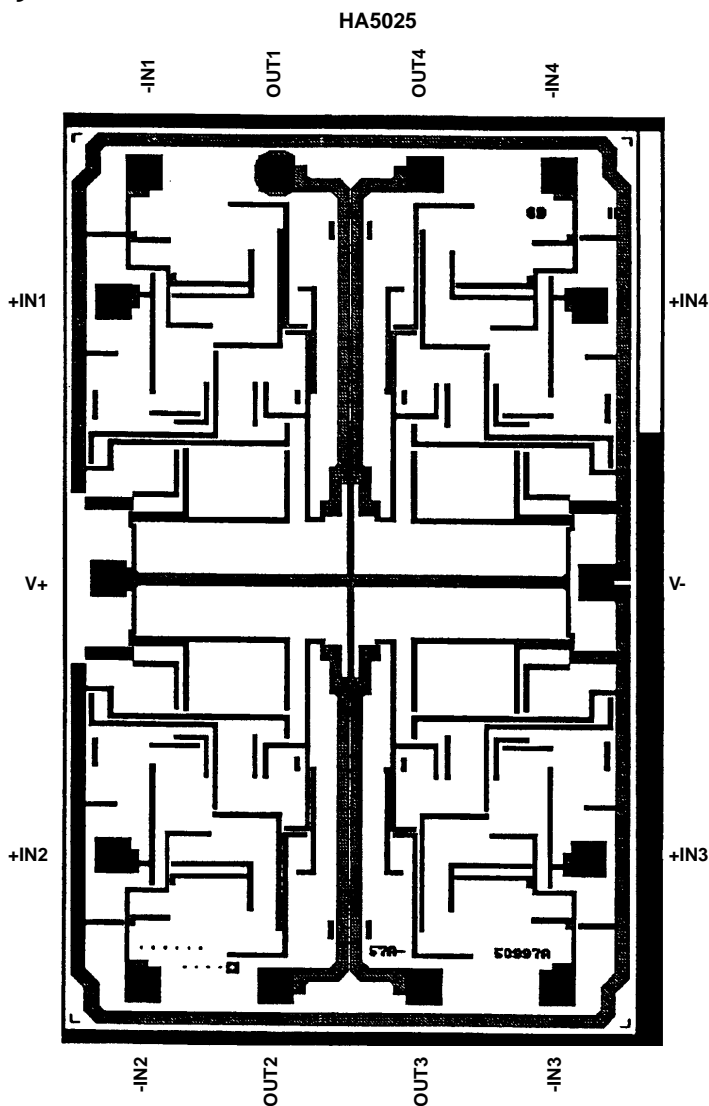
**PROCESS:**

High Frequency Bipolar Dielectric Isolation

**SUBSTRATE POTENTIAL (Powered Up):**

V-

**Metallization Mask Layout**



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